UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/655,596	09/06/2000	William F. Beausoleil	POU9-2000-0048-US1	9320

34313 7590 04/25/2003

ORRICK, HERRINGTON & SUTCLIFFE, LLP
4 PARK PLAZA
SUITE 1600
IRVINE, CA 92614-2558

EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2124	3

DATE MAILED: 04/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/655,596	BEAUSOLEIL ET AL.	
	Examiner	Art Unit	
	Tuan A Vu	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is responsive to the application filed September 6, 2000.

Claims 1-4 have been submitted for examination.

Drawings

2. The drawings are objected to because some hand-written line-drawing and element-naming are noticed for having inconsistent or fading solid lines, and/or characters, (Figs 1-2), thus rendering all relatively casual for an official document. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims are 1 rejected under 35 U.S.C. 103(a) as being unpatentable over Beausoliel et al., USPN: 5,551,013 (hereinafter Beausoliel) in view of Austin et al., USPN: 4,885,684 (hereinafter Austin).

As per claim 1, Beausoliel discloses a emulation engine comprised of a plurality of modules, a work station, and a bus for transferring data between the work station and said modules (Fig. 1,8), each of such modules including a plurality of processors and a module main memory accessible for data transfers during an emulation by each of such processors (e.g. col. 3, line 55-65; col. 5, lines 32-35; Fig. 3A-B), each of such processors having a control store to store

a programmable sequence of emulation steps that define logic states for its processor (e.g. col. 4, lines 1-5; col. 6, lines 2-10; Fig. 9A, 11A), a method to allow data transfers between such module main memory unit and work station without interrupting an in-progress emulation (*non-blocking* - col. 8, lines 16-56; Fig. 5,7), including the steps of:

compiling said programmable sequence of emulation steps to include, in at least one step, a blocking code, when the step is read from the control store (col. 10, line 64 to col. 11, line 2; col. 6, lines 2-8), as a disable command between the plurality of said processors and main memory unit (e.g. *active, inactive* - col. 6, lines 14-27, 28-59);

decoding said blocking code (e.g. col. 12, Table 1- Note: decoding is inherent to encoding instructions; Fig. 2a-b; Fig. 3a-b – Note: control word field/bit extraction is equivalent to decoding instructions code); and

transferring data between said work station and module main memory (e.g. *input to target system, emulation support facility*- col. 3, lines 28-37 ; *workstation* - Fig. 8 – Note: workstation is equivalent to host computer coordinating the support facilities functions operable on the processor modules, e.g. data or instructions transfer)

But Beausoliel does not specify a maintenance bus for transferring data between the workstation and processor modules. However, Beausoliel discloses latches and multiplexers to hold data flow to be used external to the execution of emulation logic; and path control bits multiplexing and changes for allowing concurrent data connection to support facilities (e.g. col. 3, lines 28-37; col. 8, lines 16-56; Fig. 1, 2A, 3A-B). Austin, in a network of processing units environment analogous to that of the emulating network of Beausoliel such as to use software program for deploying/supporting the functionality of the distributed data processing, discloses a

maintenance bus for both the processing elements and for the supervisor unit (e.g. *EMB* and *TM bus* - col. 6, lines 4-26) for update storage operations, and other off-line functions. In view of the suggested teachings from Beausoliel's and Austin's from above, it would have been obvious for one of ordinary skill in the art at the time the invention was made to provide a maintenance bus as taught by Austin to Beausoliel's concurrent support facilities operable within the emulation execution and operations by the processing units of Beausoliel's system because this would provide a specialized communicating channel, e.g. bus, to support the maintenance operations as suggested by Austin without affecting or interrupting the main data flow used by the processing units of the emulation by Beausoliel, thereby obviate bus/memory contention issues and enhance fault prevention, efficiency.

Nor does Beausoliel specify that in response to decoding blocking code, blocking transfers between the plurality of module processors and said module main memory units; and transferring data between the workstation and module memory units during such blocking from above. Austin, in the system for supporting and deploying distributed processors via software as mentioned above, discloses the use of maintenance bus to support the operations of the processing modules (re col. 6, lines 4-26); and teaches, via the use of LOS (Local Operating System), initialization, debug and error-related suspension operations within the emulating unit processors and/or recovery operations using such maintenance bus (e.g. col. 7, lines 51-63; *suspension, minimal overhead* - col. 12, line 47 to col. 13, line 7; *maintenance bus, alternate paths* - col. 9, lines 3-33, 42-50). Hence, in view of above-mentioned Beausoliel's teachings on support facilities and Austin's herein disclosed techniques, it would have been obvious for one of ordinary skill in the art at the time the invention was made to implement code instructions so that

when a blocking code is decoded as suggested by Beausoliel, the transferring of data between processors and their memory units is blocked so that the maintenance bus is utilized such that data can only be transferred from the central workstation onto the processors memory units just as suggested by Austin for the same reasons as mentioned above in the rejection of the maintenance bus limitation and also because this would avoid further contamination/incoherency of the processor memory when external data are written to their memory units.

As per claim 2, Beausoliel does not specify the step of unblocking transfers between the module processors memory unit when such step is sequentially decoded next after a blocking code step. But in view of Austin's teachings on suspending operations upon a failure detection (e.g. col. 7, lines 51-63; *suspension, minimal overhead* - col. 12, line 47 to col. 13, line 7; *maintenance bus, alternate paths* - col. 9, lines 3-33, 42-50) as mentioned above, it would have also been obvious to add the step of unblocking after a decoded step of blocking has been completed to Beausoliel's repetitive emulation process because the motivation would be that once the maintenance steps as suggested by Austin are completed, it would be necessary to resume the data transfer and communication between the processors and their memory unit or bus system in Beausoliel's system in order to proceed on with the rest of the emulation.

As per claim 3, Beausoliel discloses a repetitive cycle in decoding and emulating the program code (e.g. col. 12, lines 5-13) but fails to specify that the transferring of data step between module memory and workstation is repetitive. But in view of the rejection of such data transferring step as addressed in claim 1, the repetition of such data transfer would be infered from the combined teachings by Beausoliel (repetitive emulation decoding) and Austin

(maintenance bus, LOS, suspension and initialization operations) and the rejection as set forth above.

As per claim 4, Beausoliel discloses a repetitive cycle in decoding and emulating the program code (e.g. col. 12, lines 5-13) but fails to specify that the transferring of data step between modules memory units and workstation being followed by an unblocking step is repetitive. This limitation corresponds to the same limitation of claim 3 above; hence, in view of the combined teachings by Austin/Beausoliel and the rejection as set forth in claims 2, and 3 above, this limitation would have been obvious because of the rationale as set forth therein.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat No. 6,522,985 to Swoboda et al., disclosing states of emulation and path control encoded bits.

U.S. Pat No. 5,911,059 to Profit, Jr., disclosing emulation with latch control for data and interrupt watch.

U.S. Pat No. 6,480,952 to Gorishek, IV et al., disclosing host communicating with processors memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

or: (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4th Floor(Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

VAT
April 21, 2003

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100